# REMARKS

Per the undersigned's telephone conversation with the Examiner of Friday, 10 December 2004, it appears that the Office Action mailed 03 December 2004 is a duplicate of and is identical to the immediately preceding Office Action mailed 10 June 2004.

Applicants mailed on 03 September 2004 an Amendment in response to the Office Action mailed 10 June 2004. A copy of that Amendment is enclosed herewith for your convenience and reference.

Applicants respectfully request entry and consideration of the Amendment mailed 03 September 2004, and that an Office Action responsive to same be issued with a new period for response. In light of the foregoing, Applicants have not included a claims listing in this response but refer the Examiner to the enclosed copy of the Amendment mailed 03 September 2004.

In the event that Applicant has overlooked the need for an extension of time, an additional extension of time, payment of fee, or additional payment of fee, Applicant hereby conditionally petitions therefore.

The Examiner is invited to telephone the undersigned in regard to this Amendment and the above identified application

Respectfully submitted,

21-DEC-2004
Date

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PATENT
Docket: 90065.000451 (17732.6360.00)
Reply to Office Action of Jun. 10, 2004

# IN THE UNITED STATES PATENT & TRADEMARK OFFICE

Applicant: Zeng
Serial No.: 10/678,444
Filed: 01 October 2003
For: ULTRA DENSE TRENCH GATED POWER DEVICE WITH REDUCED DRAIN-SOURCE FEEDBACK CAPACITANCE AND MILLER CHARGE

Examiner: Fetsum, A.
Art Unit: 2826

# AMENDMENT

**MS: Amendment**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action mailed 10 June 2004, Applicant hereby submits the following Amendment.

# IN THE CLAIMS

1 - 13. (*Canceled*)

14. (*Currently Amended*) A method for forming a semiconductor device with reduced Miller capacitance comprising the steps of:

heavily doping a substrate with a first conductivity dopant to form a drain region;

growing an epitaxial layer on the substrate and lightly doping the epitaxial layer with a dopant of the first conductivity;

implanting the surface of the epitaxial layer with dopants of a second polarity opposite in polarity to the first conductivity dopant;

covering the substrate with a trench mask having openings corresponding to desired trench regions and removing material from the exposed regions to form trenches;

growing an oxide layer **of a substantially constant thickness** on the trench walls and floor and diffusing the second conductivity dopant to form well regions adjacent the trench sidewalls;

~~in said trench regions~~ forming **over said oxide layer on said trench walls and floor** upper and lower conductive layers and separating the layers with a first dielectric layer; **and** forming source regions in the surface of the epitaxial layer with dopant of the first conductivity.

15. (*Original*) The method of claim 14 comprising the further step of covering the wafer with a source metal region.

16. (*Original*) The method of claim 14 comprising the further step of connecting the source metal regions to the lower conductive trench layers at locations proximate the periphery of the semiconductor device.

17. (*Original*) The method of claim 14 wherein the dopant of the first conductivity is p-type and the dopant of the second conductivity is n-type.

18. (*Original*) The method of claim 14 wherein the dopant of the first conductivity is n-type and the dopant of the second conductivity is p-type.

19. (*Currently Amended*) The method of claim 14 wherein the bottom of the upper conductive layer is approximately on the same level as the bottom of the ~~of the third layer~~ well regions of second conductivity.

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20. (*Original*) The method of claim 14 wherein the dielectric layer separating the two conductive layers is silicon nitride.

21. (*Original*) The method of claim 14 further comprising the step of adding a second interlevel dielectric layer above said upper conductive layer.

22. (*Currently Amended*) The method of claim 21 wherein said second interlevel dielectric layer ~~isborophosphosilicate~~ **is borophosphosilicate** glass.

# REMARKS

Claims 14-22 are pending and rejected in the present application. Claims 14, 19 and 22 are amended hereby.

Responsive to the rejection of claim 19 under 35 U.S.C. §112, second paragraph, Applicant has amended claim 19 keeping in mind the comments offered by the Examiner. Applicant submits that claim 19 is now in allowable form, and respectfully requests withdrawal of the rejection and allowance of the claim.

As will be obvious to the Examiner, Applicant has also amended claim 22 to remove an informality therefrom.

Responsive to the rejection of claims 14-18 and 20 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,998,833 (Baliga), Applicant has amended claim 14.

To establish a *prima facie* case of obviousness, the prior art reference or references when combined must teach or suggest all the claim limitations. *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)(Emphasis Added).* Claim 14 recites in part "growing an oxide layer of a substantially constant thickness on the trench walls and floor" and "forming over said oxide layer on said trench walls and floor upper and lower conductive layers and separating the layers with a first dielectric layer". (*Emphasis Added*). Applicant submits that the cited reference fails to disclose or suggest such limitations, and that therefore a *prima facie* case of obviousness has not been established in regard thereto.

Baliga discloses in Figs. 4A-4K a method of forming a integrated power semiconductor device that includes forming trenches 20 having opposing vertical trench sidewalls 20a and trench bottom 20b. The method continues with the formation of a first electrically insulating region 24 having a first thickness of 1000-3000 Angstroms on sidewalls 20a and trench bottom 20b. (*Fig. 4d, column 9, lines 52-55*). Polysilicon region 26 (source electrode) is then formed and etched to a depth just below the second P-N junction (J2). (*Fig. 4E*). The first electrically insulating region 24 is etched and thereby removed from sidewalls 20a that are adjacent the source and drain regions 18 and 16. (*Fig. 4F, column 9, line 65 through column 10 line 5*). A second insulating layer 28 with a second thickness of 500-1000 Angstroms is formed on the exposed portions of sidewalls 20a. (*Fig. 4G*). A second polysilicon region 30 is deposited on insulating region 28 and etched to just below surface 15a (*Fig. 4H, column 10, lines 6-14*). A third insulating region 32 is formed on/over the etched polysilicon region 30. (*Fig. 4I, column 10, lines 18-20*).

Thus, Applicant submits that the method of Baliga forms no less than three separate and distinct oxide layers in the gate trench. The first layer (24, Fig. 4F) is very thick and covers a lower portion of the trench sidewalls and the trench floor; the second layer (28, Fig. 4G) is relatively thin and covers the source electrode (26) and the portion of the trench sidewalls above the source electrode; and the top layer (32) covers electrode (30).

In contrast, the present invention lines a trench with a single oxide layer having a constant thickness. This single constant-thickness oxide layer covers both the trench sidewalls and the trench bottom, and is disposed between the trench sidewalls and each of the electrodes formed therein. The three oxide layers formed by Baliga do not comprise a single oxide layer of a constant thickness, nor is any one of the three oxide layers disposed between the trench sidewalls and each of the electrodes. Further, none of the three oxide layers of Baliga line the entire trench, i.e., no single layer covers the trench walls and floor.

Thus, Baliga fails to disclose or suggest growing a single oxide layer having a constant thickness on the trench walls and floor, forming over the oxide layer on the trench walls and floor upper and lower conductive layers, and separating the layers with a first dielectric layer as recited in part by amended claim 14. Since the cited reference fails to disclose each and every limitation set forth in claim 14, Applicant submits that a *prima facie* case of obviousness has not been established in regard thereto. Accordingly, Applicant requests withdrawal of the rejection and submit that claim 14 and claims 15-22 depending therefrom are now in condition for allowance, which is hereby respectfully requested.

Further responsive to the rejection of claims 14-18 and 20 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,998,833 (Baliga), Applicant submits that the cited reference teaches away from the above-quoted subject matter recited in part by amended claim 14, and that therefore a *prima facie* case of obviousness has not been established in regard thereto.

A prior art reference that "teaches away" from the claimed invention is a significant factor to be considered in determining obviousness. *In re Gurley , 27 F.3d 551, 31 USPQ2d 1130, 1132 (Fed. Cir. 1994).* Further, it is improper to combine references where the references teach away from their combination. *In re Grasselli, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983).*

The Baliga method teaches the first insulating layer formed on the trench sidewalls and trench bottom should be relatively thick (i.e., 1000-3000 Angstroms), and that the second insulating layer formed on the portions of the trench sidewalls above the first insulating layer should be relatively thin (i.e., 500-1000 Angstroms). In short, Baliga thereby teaches it is necessary to line the lower portion of the trench with a first thick oxide layer whereas it is possible to line the upper portion of the trench with a second thinner oxide layer. Baliga thereby teaches away from the present invention, which as discussed above and as is recited in part by amended claim 14 uses a single layer of oxide having a substantially constant thickness to line the trench.

Since Baliga teaches away from the subject matter recited in part by amended claim 14, it is improper to combine or apply the reference. Therefore, Applicant submits that a *prima facie* case of obviousness has not been established in regard to claim 14. Accordingly, Applicant requests withdrawal of the rejection and submit that claim 14 and claims 15-22 depending therefrom are now in condition for allowance, which is hereby respectfully requested.

Claims 21 and 22 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,998,833 (Baliga) in view of U.S. Patent No. 5,929,482 (Kawakami, et al.). Responsive thereto, Applicant respectfully points out that claims 21 and 22 depend from claim 14, which is now in condition for allowance for the reasons provided herein. Accordingly, claims 21 and 22 are also in condition for allowance, which is hereby respectfully requested.

Claim 19, which Applicant notes was rejected under 35 U.S.C. §112, second paragraph, only and not on the basis of any prior art reference or references, recites in part "wherein the bottom of the upper conductive layer is approximately on the same level as the bottom of the well regions". (*Emphasis Added*). Applicant submits that the asserted references fail to disclose or suggest such a limitation. Accordingly, Applicant submits that claim 19 is now in condition for allowance and respectfully request same.

For all the foregoing reasons, Applicant submits that the pending claims are definite and do particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Moreover, Applicant submits that cited references fail to disclose or suggest, alone or in combination, the subject matter of the pending claims. The pending claims are therefore in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of all rejections and objections, and allowance of the claims.

In the event that Applicant has overlooked the need for an extension of time, an additional extension of time, payment of fee, or additional payment of fee, Applicant hereby conditionally petitions therefore.

The Examiner is invited to telephone the undersigned in regard to this Amendment and the above identified application.

Respectfully submitted,

2-SEPT-04
Date

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